2nd Sem VLSI

USN | | | | | | | | | | |

12EC025

M.Tech. Degree Examination, June/July 2014
Design of Analog and Mixed Mode VLSI Circuit

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Derive expression for the drain current in triode, deep triode and saturation region of MOSFET device. Also draw I_D/V_{DS} curves for these regions. **(10 Marks)**

b. Show that the output voltage varies linearly with referennce to input voltage in the case of a CS stage with diode connected load and source depenection. **(10 Marks)**

2 a. Quantify the behavior of a mos differential pair as a function of input differential voltage. **(08 Marks)**

b. In the circuit shown in Fig. 2(b) m_2 is twice as wide as m_1. Calculate the small signal gain if the bias voltages of v_{in1} and v_{in2} core equal. **(06 Marks)**

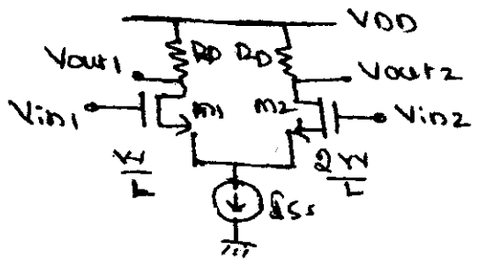

Fig. Q 2(b)

c. Calculate the small signal gain of the circuit shown in Fig. Q2(c). **(06 Marks)**

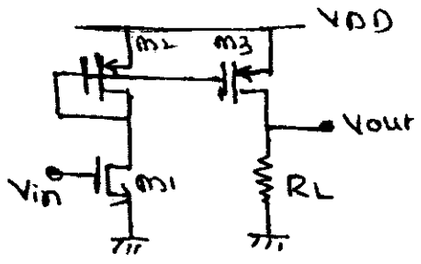

Fig. Q 2(c)

3 a. Derive expression for the input impedance of a source follower in low frequency and high frequency regions. **(10 Marks)**

b. Derive transit function of a cascade stage. **(10 Marks)**

4 a. Draw the circuit diagram of a current mirror generating output current which is independent of supply voltage and explain its operation. Also derive expression for the output current. **(08 Marks)**

b. Explain the effect of op amp off set voltage on the output voltage of bund gap reference and means to overcome the same. **(06 Marks)**

c. What is the effect of channel charge injection on the output voltage in the case of switched capacitor circuits? Explain in detail. **(06 Marks)**

5 a. Show that in a three stage ring oscillator, the minimum gain /stage =2 and $\omega_{osc} = \sqrt{3}\,\omega_0$ for oscillations to set in where ω_0 = 3dB bound width of each stage. **(06 Marks)**

b. Draw the circuit diagram of a Colpitt oscillator and explain its operation. **(06 Marks)**

c. A VCO senses a small sinusoidal control voltage $V_{cont} = V_m\omega$, ω_{mt}. Determine the output waveform and it, spectrum. **(08 Marks)**

6 a. Explain the working of a simple PLL with necessary block diagrams, wave forms, frequency and phase relations. **(10 Marks)**

b. Explain how frequency multiplication and synthesis are achieved using PLL concepts. **(10 Marks)**

7 a. Explain the working of S/H circuit with special reference to sample mode, had mode and aperture error. **(10 Marks)**

b. Explain the following specifications with reference to ADC :

i) DNL
ii) INL
iii) Off set
iv) Gain error
v) SNR. **(10 Marks)**

8 a. Explain R – ZR ladder network with necessary diagram and equations. **(10 Marks)**

b. Explain the operation of a pipeline ADC architecture, with neat diagram, **(10 Marks)**

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